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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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10/570,839

12/18/2006

Theodor Doll

3222.1430000

8784

26111 7590 04/28/2009  
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EXAMINER

SUCH, MATTHEW W

ART UNIT

PAPER NUMBER

2891

MAIL DATE

DELIVERY MODE

04/28/2009

PAPER

**Please find below and/or attached an Office communication concerning this application or proceeding.**

The time period for reply, if any, is set in the attached communication.

<b>Office Action Summary</b>	<b>Application No.</b> 10/570,839	<b>Applicant(s)</b> DOLL ET AL.	
	<b>Examiner</b> MATTHEW W. SUCH	<b>Art Unit</b> 2891	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

#### Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

#### Status

- 1) ☒ Responsive to communication(s) filed on 16 January 2009.
- 2a) ☒ This action is **FINAL**.                      2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

#### Disposition of Claims

- 4) ☒ Claim(s) 2,4,13 and 19-25 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 2,4,13 and 19-25 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

#### Application Papers

- 9) ☒ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 16 January 2009 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

#### Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All    b) ☐ Some \*    c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
  2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

#### Attachment(s)

- |  |   |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)            | 4) <input type="checkbox"/> Interview Summary (PTO-413)           |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)   | Paper No(s)/Mail Date. _____                                      |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08) | 5) <input type="checkbox"/> Notice of Informal Patent Application |
| Paper No(s)/Mail Date <u>16 January 2009</u> .   | 6) <input type="checkbox"/> Other: _____                          |

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## **DETAILED ACTION**

### ***Information Disclosure Statement***

1. The information disclosure statement (IDS) submitted on 16 January 2009 is being considered by the examiner.

### ***Drawings***

2. The drawings were received on 16 January 2009. These drawings are acceptable.

### ***Specification***

3. The specification amendments were received on 16 January 2009. These amendments are entered. However, the specification is objected to as failing to provide proper antecedent basis for the claimed subject matter. See 37 CFR 1.75(d)(1) and MPEP § 608.01(o). Correction of the following is required: inclusion of the claimed subject matter in claims 2 and 4 with the same level of detail as presented in the claims. The specification currently is vague regarding the invention without the originally filed claims and this language must be included.

### ***Claim Rejections - 35 USC § 112***

4. The following is a quotation of the first paragraph of 35 U.S.C. 112:

The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

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5. Claims 19-25 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention.

Specifically, claims 19 and 23 each require "a separation distance between the first electrode and second electrode is between ten nanometers and one hundred nanometers" and "a second electrode on the substrate and separated between ten nanometers and one hundred nanometers from the first electrode", respectively. These recitations are not supported by the specification. The specification merely reads "adjacent electrodes tightly interspaced at distances ranging between 10 nanometers and several micrometers" (See Page 1, Lines 2-3). This does not provide sufficient support for the specific elements of the first electrode and second electrode having a distance of ten nanometers and one hundred nanometers. The specification does not identify what electrodes have such a separation distance. Furthermore, there is no disclosure that the "several microns" is "one hundred nanometers".

6. The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

7. Claims 4 and 13 rejected under 35 U.S.C. 112, second paragraph, as being incomplete for omitting essential steps, such omission amounting to a gap between the steps. See MPEP § 2172.01. Specifically, claim 4 recites "applying an insulator onto the third metal layer; etching

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a portion of the insulator at the position of the first metal layer and the second metal layer".

However, this recitation renders the claims indefinite because it is unclear how a portion of the insulator at the position of the first metal layer and the second metal layer can be etched if it is never formed in the first place. The claim merely recites that the insulator is applied onto the third metal layer and fails to establish that the insulator is on the first and second metal layers.

### ***Claim Rejections - 35 USC § 102***

8. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

9. Claim 2 is rejected under 35 U.S.C. 102(b) as being anticipated by Lishan ('884).

Lishan teaches a method for producing an electronic component with closely adjacent electrodes on a substrate (Element 12, Fig. 1) comprising depositing a first metal layer (Element 10, Fig. 1) on the substrate and structuring a first photo lacquer (Element 16, Fig. 1) on a surface of the first metal layer except a portion of the surface of the metal layer wherein a portion of the surface of the first metal layer does not have the first photo lacquer thereon (see Figs. 1C and 1D, for example). The examiner notes that the usage of the term "on" in the claim does not require that the layers are in direct physical contact, and intervening layers can be therebetween. The portion of the surface of the first metal layer is etched (Para. 0007-0008; see Fig. 1E, for example) and undercut etching of the first metal layer so that an overhang is formed by the first

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photo lacquer (see Element x compared to Element x' in Fig. 1). A surface of the first photo lacquer layer is exposed to a first metal vapor so that a second metal layer (Elements 22, 24, 26, Fig. 1) is formed on the surface of the first photo lacquer and "the portion of the surface of the first metal layer (see Fig. 1F, for example) except in a space between the overhang and the substrate (see Fig. 1F without metal in the region of Element 18). The first photo lacquer and the second metal layer formed on the surface of the first photo lacquer is removed (see Fig. 1G).

***Claim Rejections - 35 USC § 103***

10. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

11. Claims 19-22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Huang ('155) in view of Scheifers ('915).

Huang teaches a bottom-gate organic transistor comprising a polymer film substrate (Element 12, Fig. 13; Para. 0023) with a first electrode source (Element 14, Fig. 13) formed on the substrate and a second electrode drain (Element 16, Fig. 13) formed on the substrate. The separation distance between the first and second electrodes is 1 micron or less (Para. 0035). A third electrode gate (Element 22, 34, Fig. 13) is formed in a hole (Element 24, Fig. 13) in the substrate in the separation between the first and second electrodes. An insulating layer (Element

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30, Fig. 13) is formed on the third electrode gate. An organic semiconductor layer (Element 28, Fig. 13) is formed on the first electrode, second electrode, and insulator.

Huang does not teach a sealing layer formed on the organic semiconductor. Scheifers teaches a conventional bottom-gate transistor with a sealing layer (Element 16) on the organic semiconductor (Element 14). It would have been obvious to one of ordinary skill in the art at the time the invention was made to use the sealing layer configuration taught by Scheifers in the device of Huang. One would have been motivated to do so since Scheifers teaches that the sealing layer protects the organic semiconductor from moisture and oxygen, thereby improving the device performance (see Abstract, at least).

While Huang teaches the separation distance between the first and second electrodes is 1 micron or less (Para. 0035), there is no explicit disclosure of 10-100 nanometers. It would have been obvious to one of ordinary skill in the art at the time the invention was made to set the dimensions between 10-100 nanometers in order to produce a small transistor size to increase the number of transistors that are packed onto a single substrate, thereby increasing processing power. The Applicant has not disclosed that the dimensions of 10-100 nanometers is for a particular unobvious purpose, produce an unexpected result, or solves any stated problem or is for any particular purpose and it appears that the invention would perform equally well if the separation were any other arbitrary value. This is supported by the fact that applicant has not disclosed any benefit for a separation of 10-100 nanometers over some other arbitrary separation distance (and, in fact, the Applicant has not even disclosed the separation of 10-100 nanometers). A change in size is recognized as being within the level of ordinary skill in the art. See, for example, *In re Rose*, 220 F.2d 459, 105 USPQ 237 (CCPA 1955); *In re Rinehart*, 531 F.2d 1048,

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189 USPQ 143 (CCPA 1976); *Gardner v. TEC Systems, Inc.*, 725 F.2d 1338, 220 USPQ 777 (Fed. Cir. 1984), cert. denied, 469 U.S. 830, 225 USPQ 232 (1984); *In re Dailey*, 357 F.2d 669, 149 USPQ 47 (CCPA 1966). Additionally, it has been held that where the general conditions of a claim are disclosed in prior art, discovering the optimum or working ranges involves only routine skill in the art. See *In re Aller*, 220 F.2d 454, 456, 105 USPQ 233, 235 (CCPA 1955).

Huang teaches that the electrodes can be formed of conductive electroplatable materials without explicitly citing the conventional materials of gold and chromium (Para. 0025). However, it would have been obvious to one of ordinary skill in the art at the time the invention was made to use either gold or chromium, since such materials provide low contact resistance and are conventional electroplatable materials and Scheifers discloses using gold for a gate, source and drain (see Para. 0025). It has been held that the selection of a known material based on its suitability for its intended use supported a *prima facie* obviousness determination in *Sinclair & Carroll Co. v. Interchemical Corp.*, 325 U.S. 327, 65 USPQ 297 (1945). See also *In re Leshin*, 227 F.2d 197, 125 USPQ 416 (CCPA 1960). MPEP § 2144.07.

12. Claims 23-25 are rejected under 35 U.S.C. 103(a) as being unpatentable over Huang ('155) in view of Scheifers ('915) in view of Higuchi (J. Poly. Sci., Part B: Poly. Phys., Vol. 34; provided as evidence).

Haung teaches a bottom-gate organic transistor comprising a polycarbonate substrate (Element 12, Fig. 13; Para. 0023, Line 5) with a first electrode source (Element 14, Fig. 13) formed on the substrate and a second electrode drain (Element 16, Fig. 13) formed on the substrate. Higuchi teaches that polycarbonate is a glass (see Higuishi who states that



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polycarbonate is a polymer glass), which is a glass that is different than  $\text{SiO}_2$  (see Higuchi "PC glasses"). The separation distance between the first and second electrodes is 1 micron or less (Para. 0035). A third electrode gate (Element 22, 34, Fig. 13) is formed in a hole (Element 24, Fig. 13) in the substrate in the separation between the first and second electrodes. An insulating layer (Element 30, Fig. 13) is formed on the third electrode gate. An organic semiconductor layer (Element 28, Fig. 13) is formed on the first electrode, second electrode, and insulator.

Huang does not teach a sealing layer formed on the organic semiconductor. Scheifers teaches a conventional bottom-gate transistor with a sealing layer (Element 16) on the organic semiconductor (Element 14). It would have been obvious to one of ordinary skill in the art at the time the invention was made to use the sealing layer configuration taught by Scheifers in the device of Huang. One would have been motivated to do so since Scheifers teaches that the sealing layer protects the organic semiconductor from moisture and oxygen, thereby improving the device performance (see Abstract, at least).

While Huang teaches the separation distance between the first and second electrodes is 1 micron or less (Para. 0035), there is no explicit disclosure of 10-100 nanometers. It would have been obvious to one of ordinary skill in the art at the time the invention was made to set the dimensions between 10-100 nanometers in order to produce a small transistor size to increase the number of transistors that are packed onto a single substrate, thereby increasing processing power. The Applicant has not disclosed that the dimensions of 10-100 nanometers is for a particular unobvious purpose, produce an unexpected result, or solves any stated problem or is for any particular purpose and it appears that the invention would perform equally well if the separation were any other arbitrary value. This is supported by the fact that applicant has not

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disclosed any benefit for a separation of 10-100 nanometers over some other arbitrary separation distance (and, in fact, the Applicant has not even disclosed the separation of 10-100 nanometers). A change in size is recognized as being within the level of ordinary skill in the art. See, for example, *In re Rose*, 220 F.2d 459, 105 USPQ 237 (CCPA 1955); *In re Rinehart*, 531 F.2d 1048, 189 USPQ 143 (CCPA 1976); *Gardner v. TEC Systems, Inc.*, 725 F.2d 1338, 220 USPQ 777 (Fed. Cir. 1984), cert. denied, 469 U.S. 830, 225 USPQ 232 (1984); *In re Dailey*, 357 F.2d 669, 149 USPQ 47 (CCPA 1966). Additionally, it has been held that where the general conditions of a claim are disclosed in prior art, discovering the optimum or working ranges involves only routine skill in the art. See *In re Aller*, 220 F.2d 454, 456, 105 USPQ 233, 235 (CCPA 1955).

Huang teaches that the electrodes can be formed of conductive electroplatable materials without explicitly citing the conventional materials of gold and chromium (Para. 0025). However, it would have been obvious to one of ordinary skill in the art at the time the invention was made to use either gold or chromium, since such materials provide low contact resistance and are conventional electroplatable materials and Scheifers discloses using gold for a gate, source and drain (see Para. 0025). It has been held that the selection of a known material based on its suitability for its intended use supported a prima facie obviousness determination in *Sinclair & Carroll Co. v. Interchemical Corp.*, 325 U.S. 327, 65 USPQ 297 (1945). See also *In re Leshin*, 227 F.2d 197, 125 USPQ 416 (CCPA 1960). MPEP § 2144.07.

### ***Response to Arguments***

13. Applicant's arguments filed 16 January 2009 have been fully considered but they are not persuasive.

14. The Applicant argues that Lishan does not teach that the first photo lacquer is not on a surface of the first metal layer (see Remarks page 10). This is not persuasive. The examiner notes that the usage of the term "on" in the claim does not require that the layers are in direct physical contact, and intervening layers can be therebetween. The Applicant argues that Lishan does not teach refraining from structuring the first photo lacquer layer on a portion of the first metal layer (see Remarks page 10). This is not persuasive. In response to applicant's argument that the references fail to show certain features of applicant's invention, it is noted that the features upon which applicant relies (i.e., refraining...) are not recited in the rejected claim(s). Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993). The Applicant argues that Lishan does not undercut etch the first metal layer and cites Para. 0007-0008 as evidence (see Remarks Page 10). This is not persuasive. In fact, the cited portions of Lishan actually teaches that the first metal layer is undercut etched so that an overhang is defined by the first photo lacquer (see the sentence, of "Another selective etchant can then be used to remove portions of the metal layer 10 where the dielectric material acts as an etching mask" and Fig. 1E shows the undercut etched first metal layer that results).

15. The Applicant argues that Huang in view of Scheifers does render obvious that a separation between the first electrode and the second electrode is between ten nanometers and one hundred nanometers (see Remarks Pages 11-12) and cites MPEP § 2144.05(III). This is not persuasive. Firstly, the Applicant's disclosure does not teach a separation between the first

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electrode and the second electrode is between ten nanometers and one hundred nanometers (see rejection under 35 U.S.C. 112, first paragraph). As shown above, it would have been obvious to one of ordinary skill in the art at the time the invention was made to set the dimensions between 10-100 nanometers in order to produce a small transistor size to increase the number of transistors that are packed onto a single substrate, thereby increasing processing power. The reference of Huang discloses 1 micron and below for the separation. The Applicant has not disclosed that the dimensions of 10-100 nanometers is for a particular unobvious purpose, produce an unexpected result, or solves any stated problem or is for any particular purpose and it appears that the invention would perform equally well if the separation were any other arbitrary value. This is supported by the fact that applicant has not disclosed any benefit for a separation of 10-100 nanometers over some other arbitrary separation distance (and, in fact, the Applicant has not even disclosed the separation of 10-100 nanometers). A change in size is recognized as being within the level of ordinary skill in the art. See, for example, *In re Rose*, 220 F.2d 459, 105 USPQ 237 (CCPA 1955); *In re Rinehart*, 531 F.2d 1048, 189 USPQ 143 (CCPA 1976); *Gardner v. TEC Systems, Inc.*, 725 F.2d 1338, 220 USPQ 777 (Fed. Cir. 1984), cert. denied, 469 U.S. 830, 225 USPQ 232 (1984); *In re Dailey*, 357 F.2d 669, 149 USPQ 47 (CCPA 1966). Additionally, it has been held that where the general conditions of a claim are disclosed in prior art, discovering the optimum or working ranges involves only routine skill in the art. See *In re Aller*, 220 F.2d 454, 456, 105 USPQ 233, 235 (CCPA 1955). Also, as noted by cited portion of MPEP § 2144.05(III), once a prima facie showing is made, the burden is on Applicant to rebut by providing evidence that the claimed range is critical. The Applicant has provided no evidence of criticality and the Applicant's arguments and assertions do not constitute evidence.

*Conclusion*

16. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure:

- i. Ostergard ('747) teaches an organic transistor with a gate electrode that is buried in the substrate
- ii. Eccleston ('486) teaches a method of forming an organic transistor by undercut etching with a photo lacquer layer.

17. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire **THREE MONTHS** from the mailing date of this action. In the event a first reply is filed within **TWO MONTHS** of the mailing date of this final action and the advisory action is not mailed until after the end of the **THREE-MONTH** shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than **SIX MONTHS** from the date of this final action.

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***Contact Information***

18. Any inquiry concerning this communication or earlier communications from the examiner should be directed to MATTHEW W. SUCH whose telephone number is (571)272-8895. The examiner can normally be reached on Monday - Friday 9AM-5PM EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kiesha Rose can be reached on (571) 272-1844. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Matthew W. Such/  
Examiner, Art Unit 2891

MWS  
4/24/09

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4/26/09